REMARKS

Claims 1-10 and 12-14 are all the claims pending in the application. Claims 11 and 15-25 are canceled, above. Claims 1-14 stand rejected on prior art grounds. Claims 3 and 9 stand rejected on informalities. Applicants respectfully traverse these rejections based on the following discussion.

I. The 35 U.S.C. 112, Second Paragraph Rejection

Claims 3 and 9 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and claim the subject matter for which applicant regards as his invention. Specifically, the Office Action asserts that the two spacers cannot be adjacent if an etch-stop layer is between them. As such, Applicants have amended claim 1, in which claim 3 depends upon, to replace "second spacers adjacent said first spacers" with "second spacers on said etch stop layer". In addition, claim 9 has been amended to replace the term "adjacent" with the term "proximate". Therefore, claims 1, 3 and 9 have been amended to particularly point out and claim the subject matter for which Applicant regards as his invention. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw these rejections.

II. The Prior Art Rejections

Claims 1, 2, and 4-7 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kao (6,500,765). Claims 3 and 8-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kao in view of Krivokapic (6,512,273). Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides an integrated circuit structure comprising first-type

transistors with first spacers adjacent first gate conductors and second-type transistors with the first spacers adjacent second gate conductors, an etch stop layer on the first spacers, and second spacers on the etch stop layer. In the rejection, the Office Action argues that Kao discloses first spacers adjacent second gate conductors, and second spacers adjacent said first spacers. In addition, the Office Action argues that Krivokapic discloses a double spacer on a p-channel device, separated by an oxide liner. However, neither Kao nor Krivokapic disclose impurity implants in areas of a substrate ***completely outside of*** the spacers. Moreover, neither Kao nor Krivokapic disclose an etch stop layer between the first spacers and the second spacers. Therefore, as explained in further detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

The Office Action argues that Kao discloses first spacers (114a) adjacent second gate conductors, and second spacers (116b) adjacent said first spacers. As illustrated in FIG. 5, Kao discloses a dielectric layer 114a adjacent a gate 106(a), and a first spacer 116b adjacent the dielectric layer 114a. However, ***Kao fails to disclose an etch stop layer.*** Such a feature is defined in independent claim 1 using the following language: "an etch stop layer on said first spacers, and second spacers on said etch stop layer." As shown in FIG. 5, the dielectric layer 114a is adjacent to the gate 106(a); and, the first spacer 116b is adjacent to the dielectric layer 114a. There is nothing between the dielectric layer 114a and the first spacer 116b.

The Office Action also argues that Krivokapic discloses a double spacer on a p-channel device, separated by an oxide liner. However, Krivokapic fails to disclose impurity implants ***completely outside of the spacers***. Such a feature is defined in independent claim 8 using the following language: "first-type impurity implants in areas of said substrate completely outside of said first spacers of said first gate conductors; and second-type impurity implants in areas of said

substrate completely outside of said second spacers of said second gate conductors." Although the specification does not explicitly state that the impurity implants are completely outside of the spacers, this is clearly shown in Figures 4, 6, 7 and 8. Therefore, Applicants' disclosure shows that the impurity implants are completely outside of the spacers.

As illustrated in FIG. 2D, the impurity implants of the Krivokapic device are directly under the spacers. More specifically, with regards to the p-channel device, greater than half of the S/D implant 37 is positioned under the spacers 20 and the spacers 33. The inner sides of the S/D implants 37 (i.e., the lateral sides closest to the gate 10) are nearly directly under the oxide liner 18, which separates the gates 10 from the spacers 20. Moreover, the entire bottom surface of spacers 33, and nearly the entire bottom surface of the spacers 20 are directly above the S/D implant 37.

Furthermore, with regards to the n-channel device, nearly half of the S/D implant 22 is positioned under the spacers 33. The inner sides of the S/D implants 22 (i.e., the lateral sides closest to the gate 10) are directly under the oxide liner 18, which separates the gates 10 from the spacers 33. Moreover, the entire bottom surface of the spacers 33, and portions of the bottom surface of the oxide liner 18 are directly above the S/D implant 22. Therefore, as FIG. 2D clearly illustrates, the impurity implants are not completely outside of the spacers.

Further unlike the claimed invention, Krivokapic does not disclose an etch stop layer. Such a feature is defined in independent claims 1 and 8 using the following language: "an etch stop layer on said first spacers, and second spacers on said etch stop layer". The second oxide liner 38 of Krivokapic does not function as an etch stop layer. Krivokapic merely discloses that "[s]econd oxide liner 38 separates nitride and poly spacers on p-channel devices." However, Krivokapic does not teach or suggest using the second oxide liner 38 as an etch stop layer.

Therefore, contrary to the position taken in the Office Action, Applicants submit that neither Kao nor Krivokapic teach or suggest an integrated circuit structure comprising first spacers, second spacers, an etch stop layer, and impurity implants completely outside of the spacers. Thus, it is Applicants' position that neither Kao nor Krivokapic disclose or suggest the claimed feature of "an etch stop layer on said first spacers, and second spacers on said etch stop layer" as defined by independent claims 1 and 8. Further, neither Kao nor Krivokapic disclose or suggest the claimed feature of "first-type impurity implants in areas of said substrate completely outside of said first spacers of said first gate conductors; and second-type impurity implants in areas of said substrate completely outside of said second spacers of said second gate conductors" as defined by independent claim 8.

Therefore, it is Applicants' position that the proposed combination of Kao and Krivokapic do not teach or suggest many features defined by independent claims 1 and 8 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 2-7, 9-10, and 12-14 are similarly patentable, not only because of their dependency from patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw these rejections.

III. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-10 and 12-14, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

Dated: 1/27/06

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